REMARKS

Each of claims 2-9, 11-13, and 20-21 stands rejected. Claims 2, 4, 8, 9, 20 and 21 are amended with this paper.

Claim 20 was objected to because line 5 of Claim 20 should have been placed before line 4. The suggested change has been made to Claim 20, obviating the objection.

Claim 2 was rejected under 35 U.S.C. §112, first paragraph. The specification has been amended to include the term "dielectric" after the term "high k" in the description of page 2, paragraph 0010. It is respectfully submitted that in the field, the term "high k" inherently means "dielectric", and hence, no new matter has been added by the amendment to the claims or to the specification. Therefore, the Applicant respectfully requests that the rejection be withdrawn.

Claims 8 and 9 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Claim 8 has been amended to recite "wherein the blocking layer comprises less than or equal to ten atomic monolayers," thereby claiming an explicit thickness for the blocking layer (see specification page 2, paragraph 11). Claim 9 contains a similar amendment for the diffusion barrier layer.

Claims 20, 3 and 4 were rejected under 35 U.S.C. §102 (e) as being anticipated by U.S. Patent Application No. 2002/0014662 to Yamazaki et al. However, Yamazaki et al. does not teach or suggest a feature recited in Claim 20, as amended, of "a diffusion barrier layer overlying the dielectric layer" (emphasis added). Support for the amended claim is found, for example, on page 3, paragraph 12. The element referred to by the Examiner as corresponding to the diffusion barrier layer, is element **15a** in Yamazaki et al., which is a polycrystalline seed layer. "The polycrystalline silicon layer **15a** is provided with a function of assisting to form the SiGe layer **15b** without effecting influence on electric properties...The thickness of the polycrystal silicon layer **15a** is, for example, about 3 nm." (page 6, paragraph [0103]). Therefore the polycrystal silicon layer is a seed layer, not a diffusion barrier. Polycrystal silicon would not normally be a barrier to dopant diffusion. Since a polycrystal silicon seed layer does not serve the same function as a diffusion barrier layer, it has different structural requirements. In particular, as a diffusion barrier, the barrier layer may be substantially thinner than the 3 nm required for the polycrystal silicon seed layer. Claim 20, as amended, is therefore patentable over Yamazaki et al. Claims 3 and 4 are patentable at least by their dependence on Claim 20.

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Dependent Claims 2, 5, and 7-9 were rejected under 35 U.S.C. §103 as being obvious over Yamazaki et al. However for at least the reasons cited above, Yamazaki et al. does not anticipate the invention as recited in base Claim 20. Therefore, Claims 2, 5, and 7-9 are patentable at least by their dependence on patentable Claim 20.

Claims 21 and 11-13 were rejected under 35 U.S.C. §103 as being unpatentable over U.S. Pat. No. 5,880,508 to Wu, in view of Yamazaki et al. However, there is no teaching or motivation in Yamazaki et al. for the use of SiGe as the material for the source/drain regions of the transistor device in accordance with Claim 21. The use of SiGe has the advantage of lowering the annealing temperature of the source/drain regions (see specification paragraphs 17 and 18) thereby increasing capacitance and reducing leakage current. In Yamazaki et al., the SiGe is used exclusively to form the gate electrode of the device, and ion implantation forms the source and drain regions in a conventional silicon (no germanium) substrate. Similarly, Wu neither teaches nor suggests any alternative technique for forming the source and drain regions of the device, other than doping silicon with conventional materials. Therefore, neither Wu nor Yamazaki et al. teach or suggest the use of SiGe as material for the source and drain regions of the transistor device. Therefore, Claim 21 is patentable over Wu in view of Yamazaki et al. Claims 11-13 are therefore patentable at least by their dependence on Claim 21.

For the above reasons, Applicant respectfully requests reconsideration and allowance of Claims 2-9, 11-13, and 20-21 all pending. Should the Examiner have any questions concerning this response, the Examiner is invited to call the undersigned at (408) 453-9200.

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Appendix A

In accordance with 37 C.F.R §1.121 (b)(1)(iii), the following is a marked-up version of the replacement paragraph with markings to show changes made.

[0010] In FIG. 3, a high k dielectric layer 21 is grown over the substrate including the implanted channel. High k dielectric layer may be, for example, a metal oxide, such as, for example, zircon oxide, titanium oxide, tantalum oxide, or hafnium oxide. The high k dielectric layer is grown epitaxially as illustrated in FIG. 9. The high k dielectric layer includes alternating monolayers of oxygen 21a and metal 21b. Epitaxial high k dielectric layer 21, and other epitaxial layers described below, may be grown, for example, by molecular beam epitaxy (MBE), chemical vapor deposition (CVD) or other epitaxial techniques. The high k dielectric layer is thick enough to have a leakage current blocking capability equivalent to a ten angstrom thick layer of SiO_2. The appropriate thickness of the high k dielectric layer can be determined as follows. The thickness of the high k dielectric layer is defined by the boundary equation $e_1E_1 = e_2E_2$, where e is a dielectric constant and E is the electric field, given by the applied bias in volts divided by the material thickness. The boundary equation therefore simplifies to $e_1/t_1 = e_2/t_2$, where t is the material thickness. For a given high k material, the required thickness can be determined by plugging in the dielectric constant of SiO_2 and a ten angstrom thickness of SiO_2 on the left hand side of the equation, plugging in the dielectric constant of the selected high k material, then solving for t_2.

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Appendix B

The following identifies the changes that the present submission makes to claims 2, 4, 8, 9, 20 and 21 of U.S. Patent Application 09/877,906 (M-11121 US).

2. (Amended) The device of Claim 20 wherein each of the dielectric layer, the [buffer] diffusion barrier layer, and the blocking layer comprise epitaxial layers.

4. (Amended) The device of Claim 20 wherein each of the [buffer] diffusion barrier layer and the blocking layer comprise silicon.

8. (Amended) The device of Claim 20 wherein the blocking layer comprises less than or equal to ten atomic monolayers [layers of atomic silicon in thickness].

9. (Amended) The device of Claim 20 wherein the [buffer] diffusion barrier layer comprises less than or equal to ten atomic monolayers[layers of atomic silicon in thickness].

20. (Amended) A semiconductor device formed on a substrate and comprising:

a well;

a channel region of first conductivity type and being in the well;

a dielectric layer overlying the channel region;

a [buffer] diffusion barrier layer overlying the dielectric layer;

[a dielectric layer overlying the channel region;]

a gate electrode overlying the [buffer] diffusion barrier layer;

a blocking layer overlying the gate electrode; and

two source/drain regions of second conductivity type formed on opposite sides of the channel region.

21. (Amended) A semiconductor device formed on a substrate and comprising:

a well;

a channel region of first conductivity type and being in the well;

a dielectric layer overlying the channel region;

a gate electrode overlying the dielectric layer; and

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two source/drain regions of second conductivity type formed on opposite sides of the channel region, wherein the source/drain regions comprise silicon germanium.

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